Preliminary Detailed Design Report (Version 2)

FPGA Enhanced Digital Beamsteering Phased Array

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I. Introduction

Problem Statement: The team needs to develop a transmitting phased antenna array that can control the main lobe of radiation by controlling the digital baseband signal.

Motivation: The motivation for beamsteering is the need for higher data transmission rates. It allows for transmission of higher quality signals to receivers. This means that the Signal to Noise Ratio is significantly higher leading to fewer errors in the transmission of data. Another upside to using beamsteering is that there is no need to increase the transmitting power in order to achieve the higher quality signal. By focusing the main lobe of the transmission radiation, we are also able to decrease the amount of interference that we inflict on other receivers because of the large attenuation in the sidelobes that comes as a by-product of beamsteering.

Requirements: The system must include an antenna array, RF up-conversion channels, digital to analog converters, and an FPGA with the optimum radiation beam control algorithm. The operating frequency needs to be within the ISM band and the output power that leads into the antenna must be less than 30 dBm. The steering angle of the beam needs to be able to have a 180 degree range.

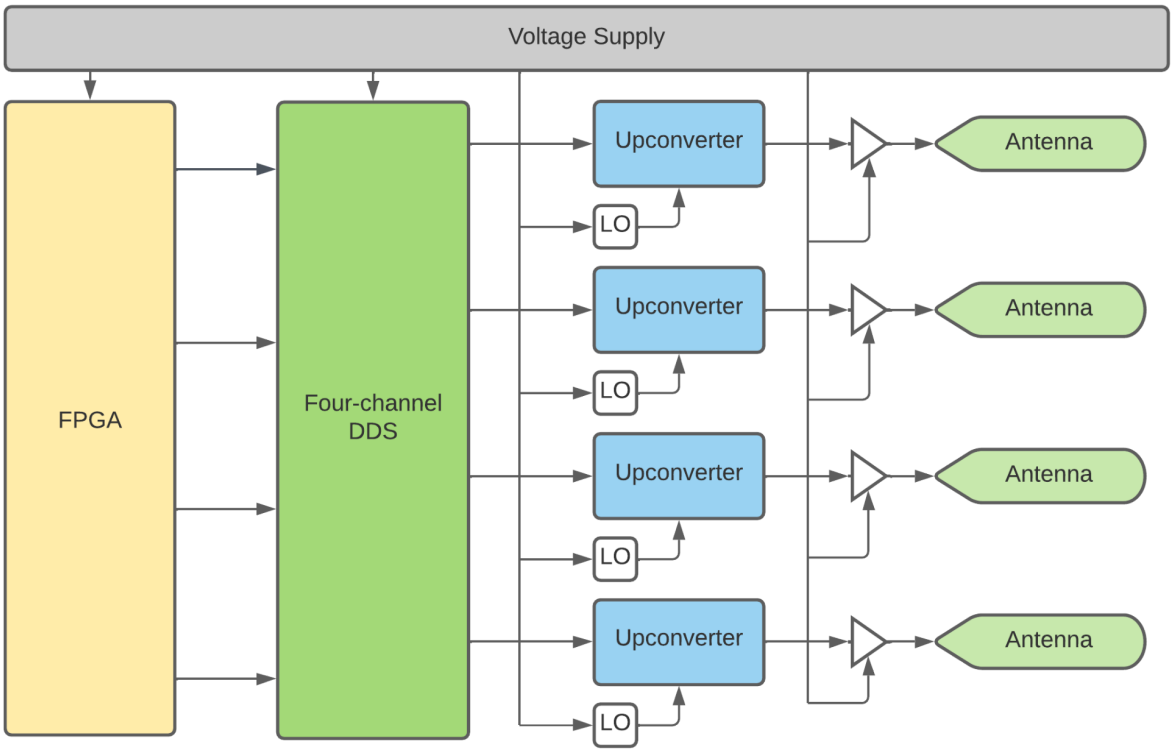
II. Selected Concept

When selecting final concepts, the first main decision was to select the type of system. Various types of systems are digitized, digital, and analog. The team has selected the digital route to implement the beam steering system. This will allow us to initially create and control the signal digitally, which later be converted to an analog signal.

We will implement a FPGA within our design. The FPGA allows us to program and control the functionality of our system. The size of the system will be handheld size. That way it can be easily transported to areas of high signal density, which may also help us when testing our final design.

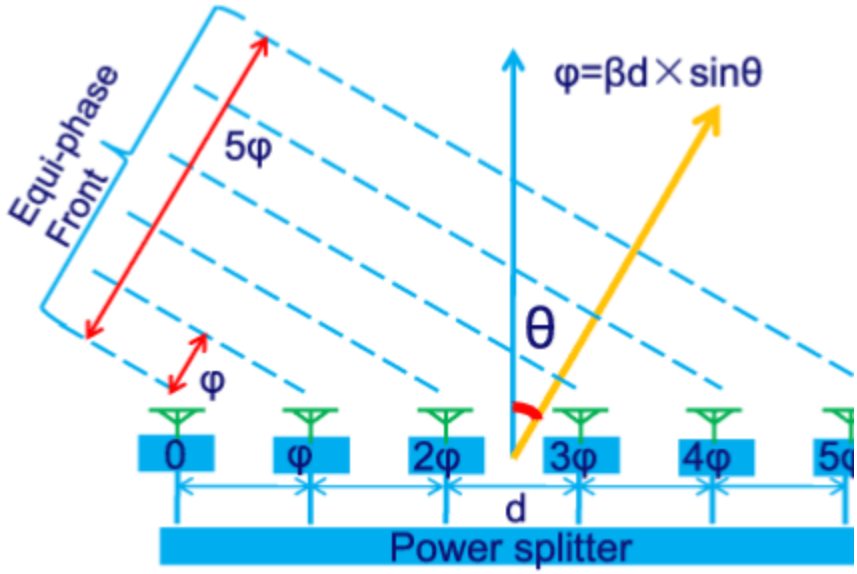
The system will initially be powered through USB port connections from our laptops. The USB connection will also allow us to upload our programs to the FPGA. Once the functionality of our system works properly, we will then implement a power source. An external power DC power supply with USB port connection will be a reliable power source to ensure power will be constantly supplied through our system.

III. Updated Preliminary Design



Voltage Supply: As previously stated, the system will initially be powered through USB port connections from our laptops. This allows us to properly upload and load our programs to the FPGA and MCU. Once we can ensure our system works as desired and the functionality of the system is perfected, we will then implement an external power source. An external power DC power supply with USB port connection will be a reliable power source to ensure power will be constantly supplied through our system. We want a reliable power source because if the power supplied to the system is interrupted at any point and time, it will affect the functionality of the system. Thus, a reliable constant power source will lead to a reliable design.

FPGA: For the project, the team is intending to use the Xilinx Spartan 6 XC6LX16-CS324 FPGA. The FPGA will take in the angle that the user wants the beam to point. The FPGA will generate a clock cycle and this output feeds into the Direct Digital Synthesizer (DDS), which will generate a sinusoidal signal for each of the channels. The FPGA will also compute the phase shift angle that the DDS needs to shift based on the input angle that the user wants the beam to point. A basic diagram relating the equation and the direction of the beam is shown below:



Where beta is 2 times pi divided by the wavelength of our frequency, which is 2.4 GHz.

Four-Channel DDS: The four channel DDS will be an AD9959 development board that consists of four direct digital synthesizers. The board will receive a reference clock signal from the FPGA that will dictate the amplitude of the base signal the four DDSs will use. Each DDS will have a separate input signal that will correspond with the required phase delay needed for each signal. The module will output four signals that will need to be amplified before being input into the antennas.

AD9959/PCBZ

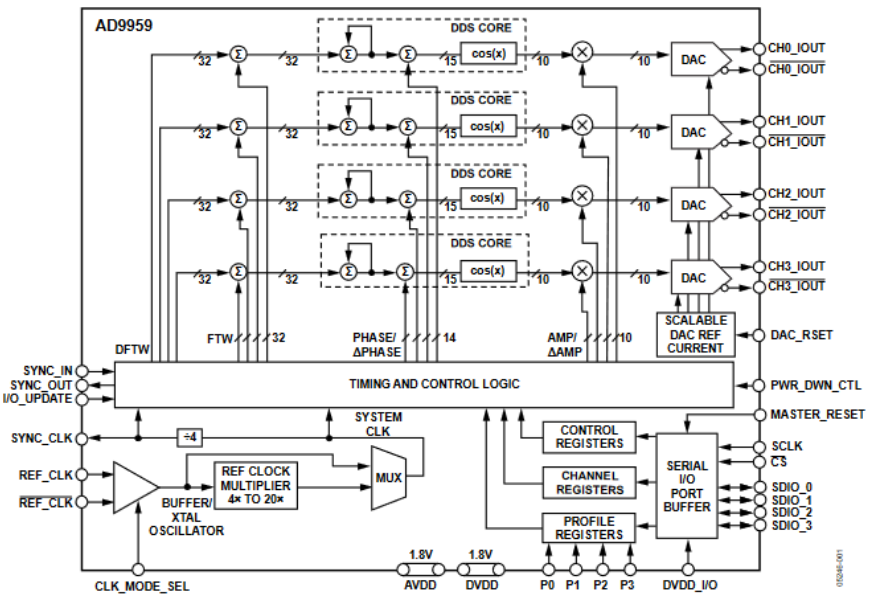
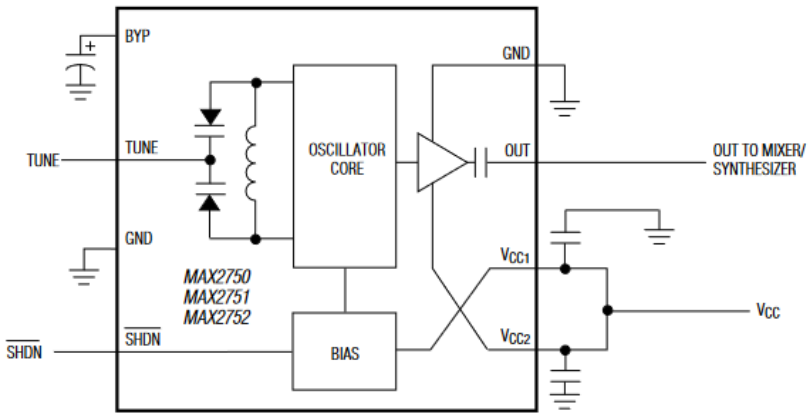


Figure 2. Detailed Block Diagram

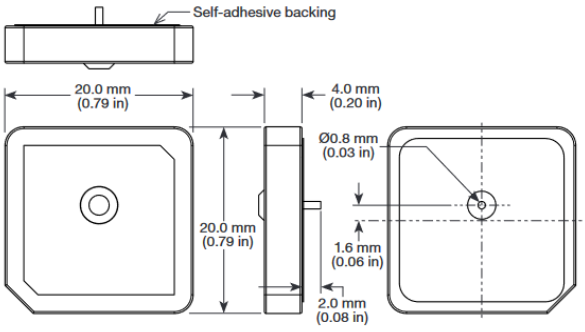
Up Converter: The upconverter will be a mixer that will combine the frequency of the signals from the DDSs with the frequency of a signal supplied by a local oscillator to reach the desired frequency.

Local Oscillator (LO): The local oscillator will be used to add the signal with the required frequency to the mixer/ upconverter. A voltage supply will supply the required input power



Amplifier Gain: A gain amplifier will be used to add power to the signal before inputting into the antenna. Power should be <30dBm.

Antenna: Four 2.4GHz patch antennas will be used. The antennas will be spaced 0.5 wavelength apart, which is about 2.46 inches from center at 2.4GHz. Since our functional decomposition we have decided to move away from using omnidirectional antennas to using directional patch antennas. Omnidirectional antennas would provide a second beam which is not needed four the purposes of this project. Directional patch antennas will be simpler to implement.



PCB: A PCB designed by the team will be used to implement the mixing and amplification of the output signal from the DDS. The PCB will consist of upconverters, local oscillators, amplifiers, voltage regulators and antennas. One of each of these components will be arranged in four circuits, one for each of the four antennas. Between each of these components will be an impedance matching network that will regulate the impedance to the 50 Ohms required for RF signals.

IV. Summary

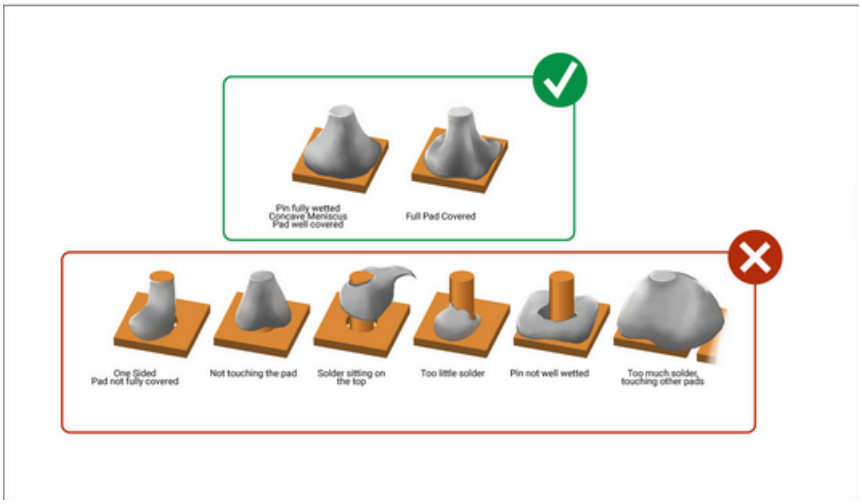
The team has selected a digital system for the project. A brief breakdown of the components for the system: The FPGA generates the clock cycles and the phase delays required for the DDS to correctly generate four signals that are offset in a way that the beam points in the direction the user intended. The upconverter takes the input from the FPGA, generates the offset signals, and converts them from digital signals to analog ones. The mixer takes the output from the DDS and the output of a local oscillator and combines them to create the designated frequency (around 2.4 GHz). The signal out of the DDS is then fed into an amplifier that adjusts the output power so that it is acceptable for the antenna.The antenna outputs the voltage based signal into a radio signal.

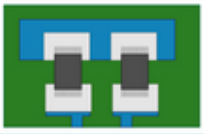
VI. Appendix

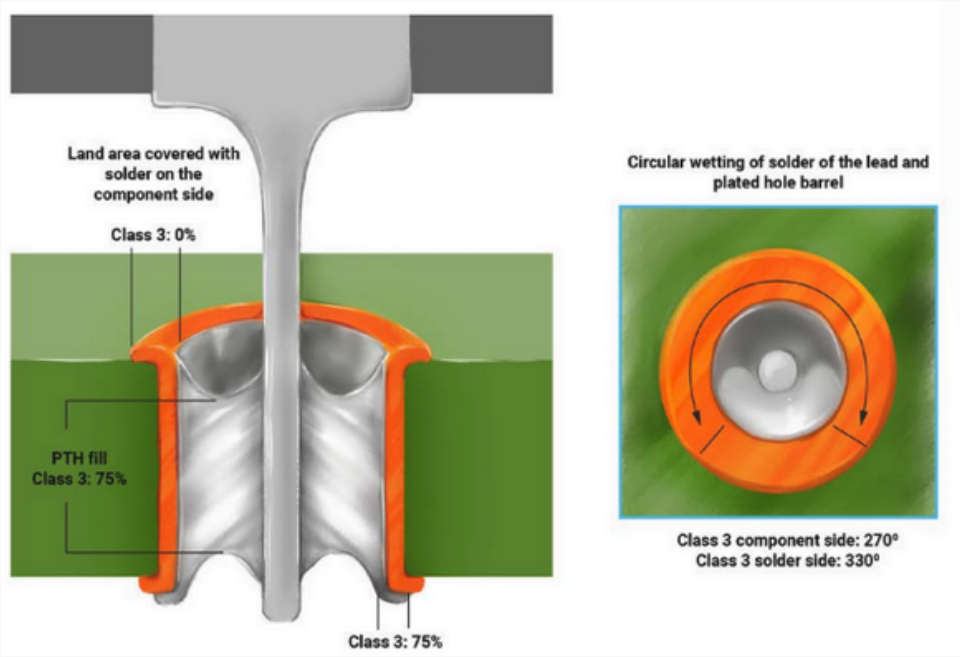
Codes and Standards:

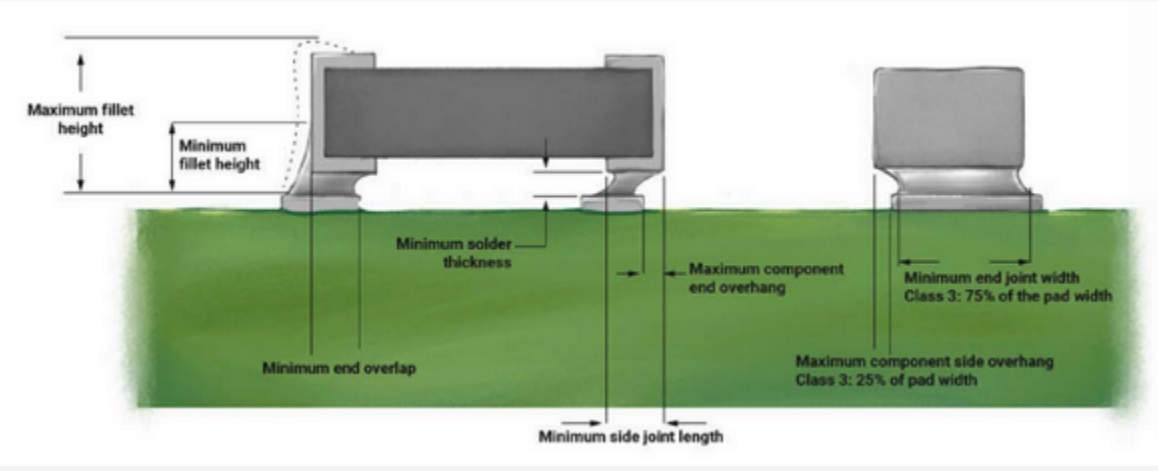
Soldering Standard IPC J-STD-001:

While soldering components to the PCB, the team will adhere to the soldering standards from IPC J-STD-001. The workspace will remain clean to prevent the contamination of materials, tools, and surfaces. The heating and cooling rates will be equivalent to the manufacturer's instructions for each component. Strands of wires will not be damaged or exposed. The solder will cover the entire tinned area of the wire. Soldering and cleanliness inspections will be conducted between each successful component soldering. If any defects may occur during soldering, the errors will be removed and re-soldered before moving on to the next component. The quality of the soldering job will meet the required specifications, shown in the images below.



Item	Poor Example	Recommended example /Separated by solder resist
Multiple parts mount		
Mount with leaded parts		
Wire soldering after mounting		
Over view		





ISM Frequency Band:

The team will adhere to the ISM Frequency Band, specifically in the 2400 - 2500 MHz range, as defined by the ITU Radio Regulation (article 5) in footnotes 5.138, 5.150, and 5.280 of the Radio Regulations. The ISM frequency band is a set of RF frequencies set aside for any purpose outside of telecommunications. It is important to stay within our range of 2400 - 2500 MHz so as to not interfere with any telecommunications systems. To operate outside of the designated ISM bands would mean a license is required. The antennas we have are rated at 2.4Ghz, which is within the ISM band we are targeting.

Referencing: IEEE 1076-2019 - IEEE Standard for VHDL Language Reference Manual

When programming the Altera FPGA, the team will closely adhere to the VHDL language standards set by the IEEE. These standards are not in place for safety reasons, but for readability of the code. The team will strive to adhere to these standards in case the code is to be read by other electrical or computer engineers in the future. The standards for VHDL are extensive, so the IEEE 1076-2019 - IEEE Standard for VHDL Language Reference Manual will be referred to periodically as the VHDL code is being written.

Public Safety and other Factors:

Project Hazard University Policy: Prior to starting an experiment, laboratory workers must conduct a project hazard assessment (PHA) to identify health, environmental and property hazards and the proper control methods to eliminate, reduce or control those hazards. PI/instructor must review, approve, and sign the written PHA and provide the identified hazard control measures. PI/instructor continually monitor projects to ensure proper controls and safety measures are available, implemented, and followed. PI/instructors are required to reevaluate a project anytime there is a change in scope or scale of a project and at least annually after the initial review. Other factors to be consider:

- Global Factors: Using 2.4 GHz because it is a globally accepted frequency in the ISM band. Emitting RF that can interfere with other devices operating in the 2.4 GHz range.
- Cultural Factors: 5G Technology is growing and often includes phased arrays.
- Social Factors: Implemented in military systems and applications.
- Environmental Factors: Can detect signals anywhere within the world as long as the signal is in the required range.
- Economic Factors: Implemented in radar transmission and detection market.